CSC332 Fall 2021 HW2 (Ch 3. Interrupts)

**Due: Wed 10/27 11 PM**

**Please write your solutions in a Word, Wordpad, or Notepad file**, and upload  **it as an attachment on Blackboard (BB).**

**Do not** directly type your answers in BB system.

**Do not send it to my email.**

**Do only one question, based on your Section (K or M) and the first letter of your last name:**

**Section K, First letter of last name A-M: Q1**

**Section K, First letter of last name N-Z: Q2**

**Section M, First letter of last name A-M: Q3**

**Section M, First letter of last name N-Z: Q4**

Q1.

At the end of a service routine, suppose we have two RTI instructions one after other. Will something go wrong? Explain.

Q2. Consider the interrupt mechanism discussed in class with the following modification. **Two new machine instructions are provided: RTIpc and RTIpsw.**

These are privileged instructions. When RTIpc is executed, it pops out the top value in the control stack and loads it onto the PC register. When RTIpsw is executed, it pops out the top value from the control stack and loads it onto the PSW register.

**When an interrupt occurs**, as discussed in class, PC and PSW values are pushed onto the control stack. **Assume that they are pushed in the right order so that PC is at the top and PSW is just below it.**

**Assume that the logical and physical addresses are same.**

There are no other changes to the interrupt mechanism that we discussed in class.

Suppose we take a correctly working service routine, written along the lines discussed in class. Now we replace its RTI instruction by the **two instruction sequence:**

**RTIpc**

**RTIpsw**

**Will the new code work correctly?**

Explain in LESS THAN 100 WORDS.

Q3.

Below we give an argument to show that the interrupt mechanism (cpu hardware + service routine actions) does not work correctly. Do you agree with the argument? If not, then what is wrong with the argument?

The argument:

Suppose we have a user program fragment:

L1: CMP R1, R2

L2: Jmpn L3

…

…

L3:

Now suppose there is a hardware interrupt after executing L1 instruction. Suppose that service routine changes condition codes. So when we come back to execute L2, the Jmpn will not work correctly.

Q4. Consider a DIV instruction: DIV R1, R2

Assume that it divides R1 by R2 and puts the quotient in R1. Condition codes are set as usual. If value of R2 is zero, then that generates an interrupt that dumps the program.

In the machine language, suppose we create a similar instruction which is a system call SYSDIV used like: SYSDIV R1, R2

The service routine for SYSDIV is:

if (value of R2)==0 then dump the user program

else DIV R1, R2;

RTI

Would you say that any old user program with DIV instruction will continue working in the new machine if we simply replace any DIV instructions in this old program by SYSDIV? Explain.